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	Application No.	Applicant(s)
Notice of Allowability	09/677,698	NAIR ET AL.
	Examiner	Art Unit
	Steven H. Rao	2814
The MAILING DATE of this communication appear All claims being allowable, PROSECUTION ON THE MERITS IS (herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGORY OF THE OFFICE	OR REMAINS) CLOSED in this or other appropriate communicated GHTS. This application is subjection.	application. If not included tion will be mailed in due course. THIS
1. This communication is responsive to <u>03/29/04</u> .		
2. The allowed claim(s) is/are <u>2-7 and 20-23</u> .		
3. \boxtimes The drawings filed on <u>05 March 2003</u> are accepted by the E	Examiner.	
4.		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO-1449 or PTO/SB/06 Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview Summ Paper No./Mail 8), 7. ☐ Examiner's Ame	Date

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Response to Amendment

Applicants' supplemental Appeal brief filed on March 29, 2004 and the Amendment after final filed 11/24/ 2003 has been entered.

Therefore claims 2 to 7 and 20 as amended by the 116 amendment and claims 21-23 as recited in the 116 amendment are currently pending in the Application.

Claims 1 and 8 to 19 have been cancelled.

Reasons for allowance

Claims 2-7 and 20-23 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitation of the dependent claims, in such manner that a rejection under 35 U.S.C. 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in independent claims, which an apparatus, comprising: a metal-oxide-semiconductor transistor having a metallic gate electrode coupled to a diffused gate region of said metal-oxide-semiconductor transistor and to a positive power supply voltage source trace; and a metallic source electrode and a metallic drain electrode coupled to said metal-oxide-semiconductor transistor and to each other and to a negative power supply voltage source trace, wherein said metal-oxide- semiconductor transistor includes the diffused gate region formed from material with a work function less than - 0.56 volts.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRIMARY EXAMINER

Steven H Rao

Patent Examiner

September 02, 2004.